CMOS Voltage Reference Design using Variable-Voltage Charge-Pump Circuit

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Abstract: This paper presents design of CMOS voltage reference circuit, by replacing the analog amplifier in the conventional CMOS voltage reference circuit with a low-voltage comparator, a charge-pump circuit with extended voltage range, and a digital control circuit with minimum supply voltage. The reference voltage circuits are used to adjust the clock frequency to regulate the charge pump to a steady output voltage under a large range of current loads. The parameters such as output resistances and power conversion efficiencies are the performance measures of charge pumps circuits. The propose circuits are design using transmission gate logic. Using transmission gate maximum voltage range is expected and no longer limited by the breakdown voltages of the devices.

Keywords: - Microwind, Auxiliary Amplifier, PLL, Charge-pump circuit, Control Circuit Unit, Low Voltage Comparator, CMOS Voltage Reference, Sub-Threshold Voltage.

I. INTRODUCTION

Power dissipation is the major concern of very large scale integration circuits. As the transistor size (channel length, width, oxide thickness etc.) reduces the interfaced circuits requires low voltage power supply whereas many circuits such as Flash memories, DRAMs and drivers of speakers and displays require higher voltages to function correctly. VLSI circuits require a precise and stable reference supply voltage circuit. A large range of voltage reference circuits is design, but they cannot work at supply voltage less than the threshold voltage due to analog circuits. A CMOS voltage reference circuit, by replacing the analog amplifier in the conventional CMOS voltage reference circuit with a low-voltage comparator, a charge-pump circuit with extended voltage range, and a digital control circuit with minimum supply voltage. They can be fabricated on the chip of the digital and analog circuits to achieve less area and lower cost. A charge pump logic in reference voltage circuit is use as voltage converters to convert variable DC voltage from a DC power supply. It uses a capacitors to pass the electric charge from one stage to the next stage, pump the voltage art output node to a higher or lower potential. The charge transfer between capacitors is controlled by switches.

II. RELATED WORK

In the base paper they proposes a sub- threshold CMOS voltage reference circuit, which reduces the minimum supply voltage by replacing the analog amplifier in the conventional CMOS voltage reference circuit with a low-voltage comparator, a charge-pump circuit, and a digital control circuit. There sub- threshold designed CMOS voltage reference circuit, is based on the conventional CMOS voltage reference circuit. The circuit reduces the supply voltage by replacing the analog amplifier to a low voltage comparator, a charge-pump circuit, and a digital control circuit operating at the supply voltage under the threshold voltage. It reduces the minimum required supply voltage by replacing the analog amplifier with the low-voltage comparator, charge-pump circuit, and digital control circuit [1].

Charge Pump Logic:

Charge pumps use a technique to transfer charge from a first capacitor to a second capacitor. The first capacitor called as transfer capacitor is charged by analog switches to the supply voltage level and then transfer this charge to the second capacitor called as storage capacitor connected to output voltage. The first capacitor is then charged again and the cycle repeats. Thus Charge pumps use capacitors as energy storage elements and pump the charges towards the output using switches to generate high DC voltage from the low DC voltage [2, 3].

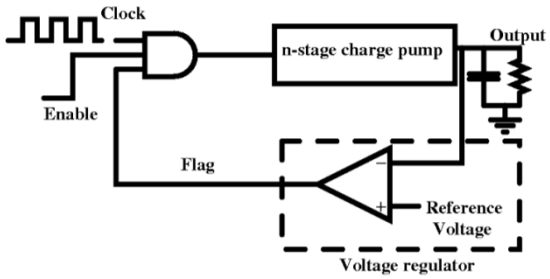

Fig 1 Basic Charge Pump Logic.

As shown in fig 1, let consider the output of charge pump logic is at zero level and the feedback will enable the charge pump circuit. The comparator is use the made activate or deactivate the charge pump logic circuit by comparing the output voltage with the reference voltage. When the charge pump circuit activates, it increase the output voltage equal to the regulated voltage level. Then the voltage regulator turn off the charge pump circuit. This charge pump output remains constant for long time due to the capacitive load. Due to coupling effects and leakage power, the output of the charge pump will discharge with time. This causes
the output voltage to go below the regulated level, which results in enabling of the charge pump by the voltage regulator, and the process keeps on repeating [2,3].

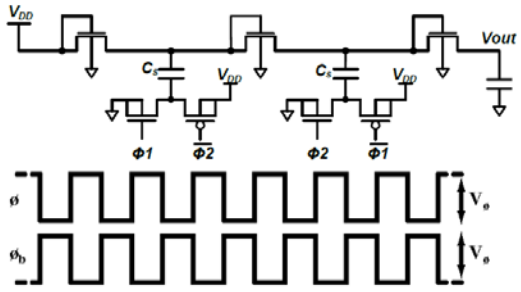

Fig 2: charge pump with NMOS transistors.

The charge pump structure has shown in fig 2 uses the chain of capacitor with two non-overlapping clock signals to generates the output load capacitor voltage. This non-overlapping clock reduces the CMOS driver current. The switching between the capacitors is controlled by NMOS transistor connected in saturation mode, which are turned on when the anode voltage is higher.

Charge Pump logic use in PLL:

Charge pump (CP) use in phase lock loop (PLL) converts the phase or frequency difference information of two input signal into a voltage which is used to tune a "Voltage Controlled Oscillator" toward reference input frequency. Other elements of PLL are "Phase Frequency Detector (PFD)", "Low Pass Filter (LPF)" and "Voltage Controlled Oscillator (VCO)". Implementation of LPF is very easy while PFD and VCO can be implemented in static CMOS logic. But being a current driven system, charge pump finds to be more challenging for implementation, since performance of CP directly affects the speed, power consumption and noise behaviour of PLL. Clock feed through, charge sharing, current mismatch are some of the challenges in design of CP.

Op-amp as a Comparator:

A two-stage CMOS op-amp is used in this ADC, as it is one of the most widely used and best understood op-amps. The core of the operational amplifier is the differential amplifier, so the chosen circuit layout is very influential on the overall performance of the op-amp. The technology employed is UMC 0.12 mm which consists of a p-substrate. Therefore a p-channel diff amp similar to that in fig. was chosen. The reason for this is that a PMOS created using a p-substrate is more insensitive to bulk effects than an equivalent NMOS. If the situation was converse to this then an n-channel diff amp would be better suited. The bulk effect varies the MOSFET threshold voltage VT and occurs when the substrate voltage of the transistor is not the same as the source voltage. When this occurs the problem is that the polarity of the PN junction that exists between the bulk and the source can be altered. If it becomes forward biased then the transistor doesn't function properly. If it remains reverse biased the depletion region increases. A larger depletion region means that a larger charge will have to be applied to overcome it. Hence VT has increased. To eliminate this bulk effect in the differential transistors, PMOSs are used, so the situation can't arise where the junction between the source and the bulk is forward biased.

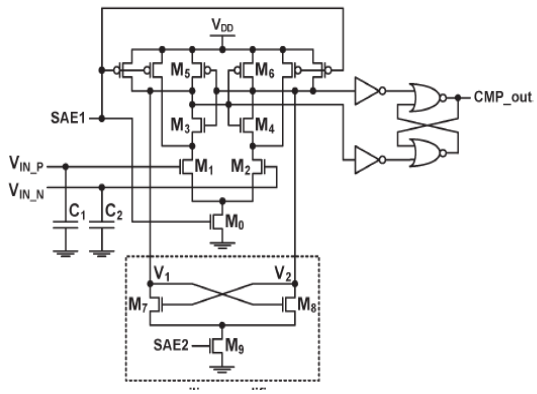

Fig Op-amp as a Comparator

The higher the op-amps gain the more linear the ramp will be. The gain of the two stage op-amp is determined by both the gain of the diff amp stage and output stage. The first stage gain is given by Av = gm (Ron). The speed at which the differential amp can operate at is directly related to its slew rate. The slew rate of the differential amplifier is dependent on the value of the current ISS (which is determined by the current source) and also the capacitance from the output node to ac ground. Basically it can be expressed as:

Slew rate α I /C

Where C is the total capacitance connected to the output node (this includes the compensation capacitor CC) and I is the current source current magnitude. Another important factor in the comparators design is the comparators resolution. The comparator needs to be able to distinguish voltage differences to within 1 LSB of accuracy, in this case 9.4 mV. The resolution of the comparator is determined by the gain of the comparator i.e. the gain of both stages. Increasing the current to increase the comparators response time also helps to improve the resolution at the expense of increased power consumption.

Current Mirror

We know that without effective biases & references no circuit & voltage sources affect power consumption, speed, dynamic range & noise performance.

As the name itself suggests a current mirror is used to generate a replica of a gain reference current. It use look at the electric function of the circuit, a current mirror is a current controlled current source (cccs).

The current gain factor can only be positive while the output impedance, the dynamic range & the speed are finite.

Moreover, the current gain to be copied is not measured ideally as it would be necessary.

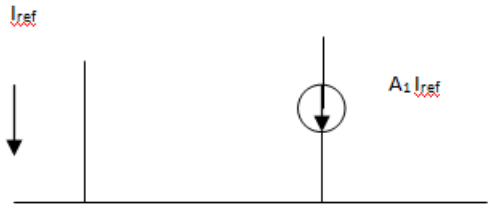

Figure 2: Equivalent circuit of an ideal current mirror.

This circuit consist of a branch that measure the reference current & the cccs. In real circuits, current mirror are not able to accomplish the function of a cccs exactly.

Current mirror is composed of two transistors of which one, M_1, is diode- connected.M_1 receives the reference current I_{Ref} & measures it by developing at its gate voltage V_{GS}; the biases the gate of M_2.

Since $V_{GS1}=V_{GS2}$, ideally the same current, or a multiple of the current in M_1, flows through M_2. If the MOSFET are the same size, the same drain current flows in each MOSFET, provided M_2 stays in the saturation region. The current I_{D1} is given by

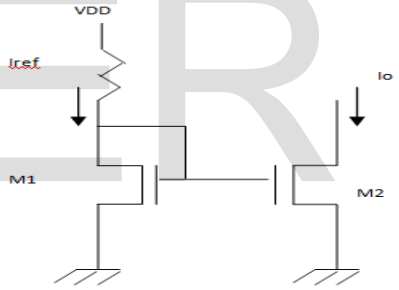

Fig 3: Schematic of NMOS current mirror circuit.

$$I_{D1} = \frac{\beta_1}{2}(V_{GS1} - V_{THN})^2$$

While the output current, flowing in M2 is

$$I_{D2} = I_0 = \frac{\beta_2}{2}(V_{GS2} - V_{THN})^2$$

Since $V_{GS2} = V_{GS1}$, the ratio of the drain current is given by

$$\frac{I_{D2}}{I_{D1}} = \frac{W_2 / L_2}{W_1 / L_1} = \frac{W_2 L_1}{W_1 L_2} = \frac{\beta_2}{\beta_1}$$

This equation (1.26) shows how to adjust the W/L ratio of the two devices to achieve the desired output current I_{D2}. This equation however does not show how the output current will change with the voltage across M_2, V_O .The reference drain current, I_D, in fig [1.17] is determined by solving

$$I_{D1} = \frac{V_{DD} - V_{GS} - V_{SS}}{R}$$

The minimum voltage, v_{min}, across the current sink is set by the requirement that M_2 remain in saturation, that is

$$V_{\min} = V_{DSAT} = V_{GS} - V_{THN}$$

The output resistance of the current source is simply the output resistance of M_2, or

$$r_{02} = \frac{1}{\lambda I_0} = \frac{1}{\lambda I_{D2}}$$

When designing CMOS current mirrors, the values for V_{GS} & L are selected before solving for w to get the desired current. Picking the lengths of all MOSFETs, used in current sources, the same size.

$$\frac{I_{D2}}{I_{D1}} = \frac{W_2}{W_1}$$

Simple Phase Locked Loop

The implementation of the PLL schematic shown in fig [1.21].Notice that the resistor R_{filter}(1000Ω) and R_{vdd2}(5000Ω) have been implemented using virtual elements and not physical resistance. The same can be said for the capacitor C_{filter} (0.3pF).However the resistance and capacitance are easy to integrate on chip.

The input frequency is fixed to 10.5GHz. During the initialization phase the pre-charge is active. This rapidly pushes the voltage of V_c to around $V_{DD}/2$.The VCO oscillation is started and the phase detector starts operating erratically.

The x-nor is an interesting indication of what happens inside the phase detector. We see that the phase difference is very important during the first 10 n sec. Then, the VCO output starts to converge to the reference clock. In terms of voltage control, V_c tends to oscillate and then converge to a stable state where the PLL is locked and stable .The output is equal to the input, and the phase difference is equal to one fourth of the period ($\pi/2$) according to the phase detector principles [3].

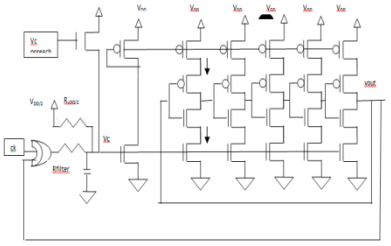

Fig 4: Schematic diagram of simple PLL.

III. CONCLUSION

The purpose of this work is design of low reference voltage generated stable DC to low and high voltage level converter circuit. A sub- threshold CMOS voltage reference circuit has been discussed. This circuit is based on the CMOS voltage reference circuit operating at a low supply voltage. It reduces the minimum required supply voltage by replacing the analog amplifier with the low-voltage comparator, charge-pump circuit, and digital control circuit.

IV. REFERENCES

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